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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,348	02/24/2004	Scott J. DeBoer	1999-1335.01/US	4548

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EXAMINER	
PHAM, HOAI V	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,348	DEBOER ET AL.	
	Examiner	Art Unit	
	Hoai v. Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03/10/2005*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,15-19,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,15-19,21 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/24/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-5 and 15-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Noble [U.S. Pat. 6,190,960] previously applied.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

**Notice: as interpreting the claim in a broad scope, a dielectric etch stop liner can also be the same as a dielectric spacer because the claim does not recite the different material between the dielectric etch stop liner and the dielectric spacer.

With respect to claim 1, Noble (fig. 17, cols. 6-10) discloses a semiconductor device comprising:

first and second contact pads (1530, 1531);

a first plug portion (1010) electrically coupled with the first contact pad (1530);

a capacitor bottom plate (1001) electrically coupled with the second contact pad (1531);

a dielectric etch stop liner (800) interposed between the bottom plate (1002) and the first plug portion (1010);

a dielectric spacer (800) (an inner portion of layer 800) interposed between the dielectric etch stop liner and the first plug portion and contacting the dielectric etch stop liner and the first plug portion;

a capacitor top plate (1210) having a portion which at least partially extends over the etch stop liner, wherein the top plate portion is farther from the first contact pad than a top surface of the first plug portion, and wherein the top plate has an opening therein; and

a second plug portion (1510) electrically coupled with the first plug portion (1010) and extending through the opening in the top plate.

With respect to claim 2, Noble (fig. 17, col. 10, lines 1-5) further discloses that a dielectric spacer (800) is a first dielectric spacer and the semiconductor device comprises a second dielectric spacer (1500) which electrically separates the second plug portion (1510) from the capacitor top plate portion (1210).

With respect to claim 3, Noble (fig. 17) discloses that the bottom plate comprises, in cross section, at least two vertically-oriented portions which define a container, wherein at least part of each vertically-oriented portion of the bottom plate is interposed between two vertically-oriented portions of the top plate and is separated by the two vertically-oriented portions of the top plate by a capacitor cell dielectric layer to form a double-sided container capacitor.

With respect to claim 4, Noble (fig. 17) further discloses that a capacitor cell dielectric layer (1200) which contacts the etch stop liner (800) and the capacitor top plate (1210).

With respect to claim 5, Noble (fig. 17) further discloses that a receptacle defined by said capacitor top plate (1210), wherein the receptacle is interposed between the first plug portion (1010) and the capacitor bottom plate (1001).

With respect to claim 15, Noble (fig. 17, cols. 6-10) discloses a semiconductor device comprising:

first and second conductive storage capacitor bottom plates (1001, 1002) each comprising a vertically-oriented sidewall;

a conductive plug (1010) interposed between the first and second conductive storage capacitor bottom plates (1001, 1002);

a first cross-sectional etch stop liner (800) interposed between the first conductive storage capacitor bottom plate and the conductive plug and a second cross-sectional etch stop liner (800) interposed between the second conductive storage capacitor bottom plate and the conductive plug;

a first cross-sectional dielectric spacer (800) (an inner portion of layer 800) interposed between the first cross-sectional etch stop liner and the conductive plug and a second cross-sectional dielectric spacer interposed between the second cross-sectional etch stop liner and the conductive plug; and

a conductive storage capacitor top plate (1210) comprising an opening therein and further comprising first and second vertical surfaces which define a first receptacle and third and fourth vertical surfaces which define a second receptacle,

wherein the first receptacle is interposed between the first conductive storage capacitor bottom plate (1101) and the conductive plug (1010), and the second receptacle is interposed between the second conductive storage capacitor bottom plate (1002) and the conductive plug (1010).

With respect to claim 16, Noble (fig. 17) further discloses that the conductive plug (1010) is a first portion of a conductive plug and the semiconductor device further comprises:

a second portion of the conductive plug (1510) electrically connected to the first portion of the conductive plug, wherein the second portion of the conductive plug passes through the opening in the capacitor top plate (1210).

With respect to claim 17, Noble (fig. 17) further discloses that the first cross-sectional etch stop liner is interposed between the first receptacle of the conductive storage capacitor top plate and the conductive plug and the second cross-sectional etch stop liner is interposed between the second receptacle of the conductive storage capacitor top plate and the conductive plug.

With respect to claim 18, Noble (fig. 17, cols. 6-10) discloses a semiconductor device comprising:

first and second digit line contact plug portions (1010, 1510), wherein the second digit line plug portion (1510) overlies and electrically connects with the first digit line plug portion (1010);

a container capacitor bottom plate (1001) having first and second vertically-oriented, cross-sectional sidewalls and a horizontally-oriented bottom electrically connected with the first and second sidewalls, wherein the first and second sidewalls and the bottom define a receptacle and the vertically-oriented sidewalls each having a first surface inside the receptacle and a second surface outside the receptacle;

a container capacitor top plate (1210) having a first vertically-oriented surface inside the receptacle and second and third vertically-oriented surfaces outside the receptacle, wherein the first and second vertically-oriented surfaces of the top plate are separated from the first vertically-oriented sidewall of the bottom plate by only a capacitor cell dielectric layer (1200) and wherein the second and third surfaces of the

top plate, together with a bottom horizontally-oriented surface of the top plate, define a receptacle;

an etch stop liner (800) interposed between the first digit line contact plug portion and the container capacitor bottom plate; and

a dielectric spacer (800) (an inner portion of layer 800) interposed between the etch stop liner and the first digit line contact plug portion.

With respect to claim 19, Noble (fig. 17) further discloses that the capacitor top plate (1210) having a hole therein wherein the second digit line plug portion (1510) passes through the hole in the capacitor top plate.

With respect to claim 20, Noble (fig. 17) further discloses that a dielectric liner (800) interposed between the first digit line plug portion (1010) and the receptacle defined by the capacitor top plate (1210).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 6 and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble [U.S. Pat. 6,190,960] previously applied.

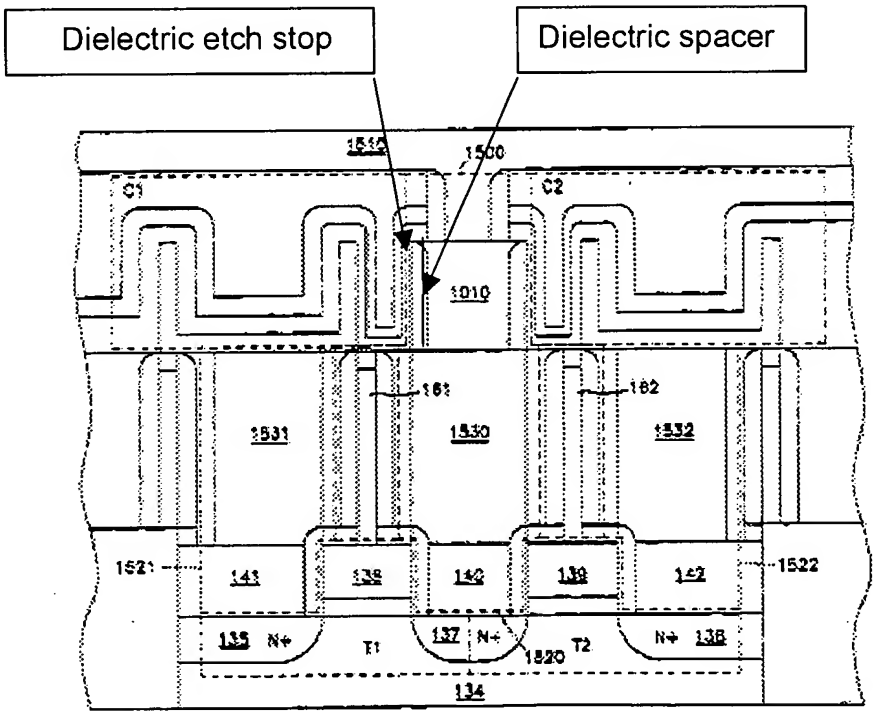
Noble does not teach the height range of the receptacle and the capacitor top plate, as claimed by Applicant. However, the height range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, it appears that these changes produce no functional differences and therefore would have been obvious. See *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

6. Applicant's arguments filed 3/10/2005 have been fully considered but they are not persuasive.

Applicant argues that Noble fails to teach or suggest "a dielectric spacer interposed between the dielectric etch stop liner and the first plug portion and contacting the dielectric etch stop liner and the first plug portion".

Applicant's argument are not persuasive because the claim does not recite the different material between the dielectric etch stop liner and the dielectric spacer. Therefore, the dielectric etch stop liner and the dielectric spacer can be considered as one layer.



Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

8. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai v. Pham whose telephone number is 571-272-1715. The examiner can normally be reached on M-F.

10. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAI PHAM
PRIMARY EXAMINER